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H4L LECTH L215

(56) Documents Cited
WO 2002/025826 A2
WO 1997/029553 A1
WO 1997/015913 A1
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US 5594672 A
US 5477476 A

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(54) Abstract Title
**Power saving in a peripheral device**

(57) A communications system comprises a PDA 1 and a Bluetooth (RTM) peripheral device 3. The Bluetooth peripheral device 3 has an antenna 5 attached thereto and is connected to the PDA 1 by means of a data channel 7. The Bluetooth peripheral device 3 enables the PDA 1 to communicate with remote data networks using the Bluetooth wireless protocol. The system is configured to operate according to an algorithm that enables the Bluetooth peripheral device 3 to enter an ultra-low power mode in which clock devices associated with data transfer (or receiving means) can be disabled when no data, or less than a predetermined amount of data, is required to be transmitted. Data loss is prevented through the use of a hardware handshake mechanism which stop the PDA 1 from sending data whilst the Bluetooth peripheral device 3 is in the low power mode. Latency in the PDA 1 responding to a change in handshake signals is catered for.

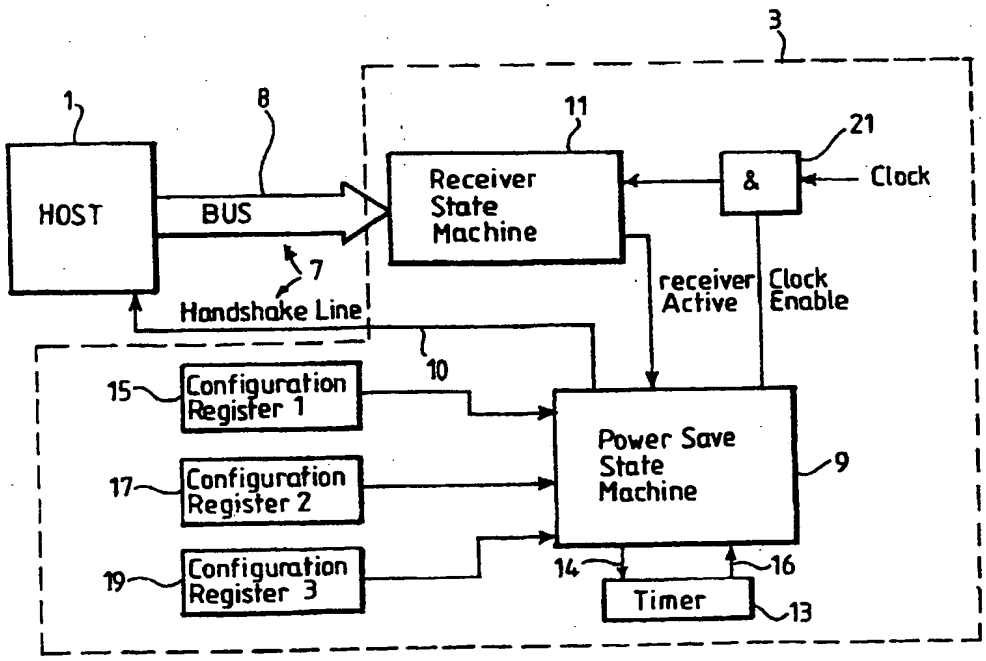


Fig.2.

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At least one drawing originally filed was informal and the print reproduced here is taken from a later filed formal copy.

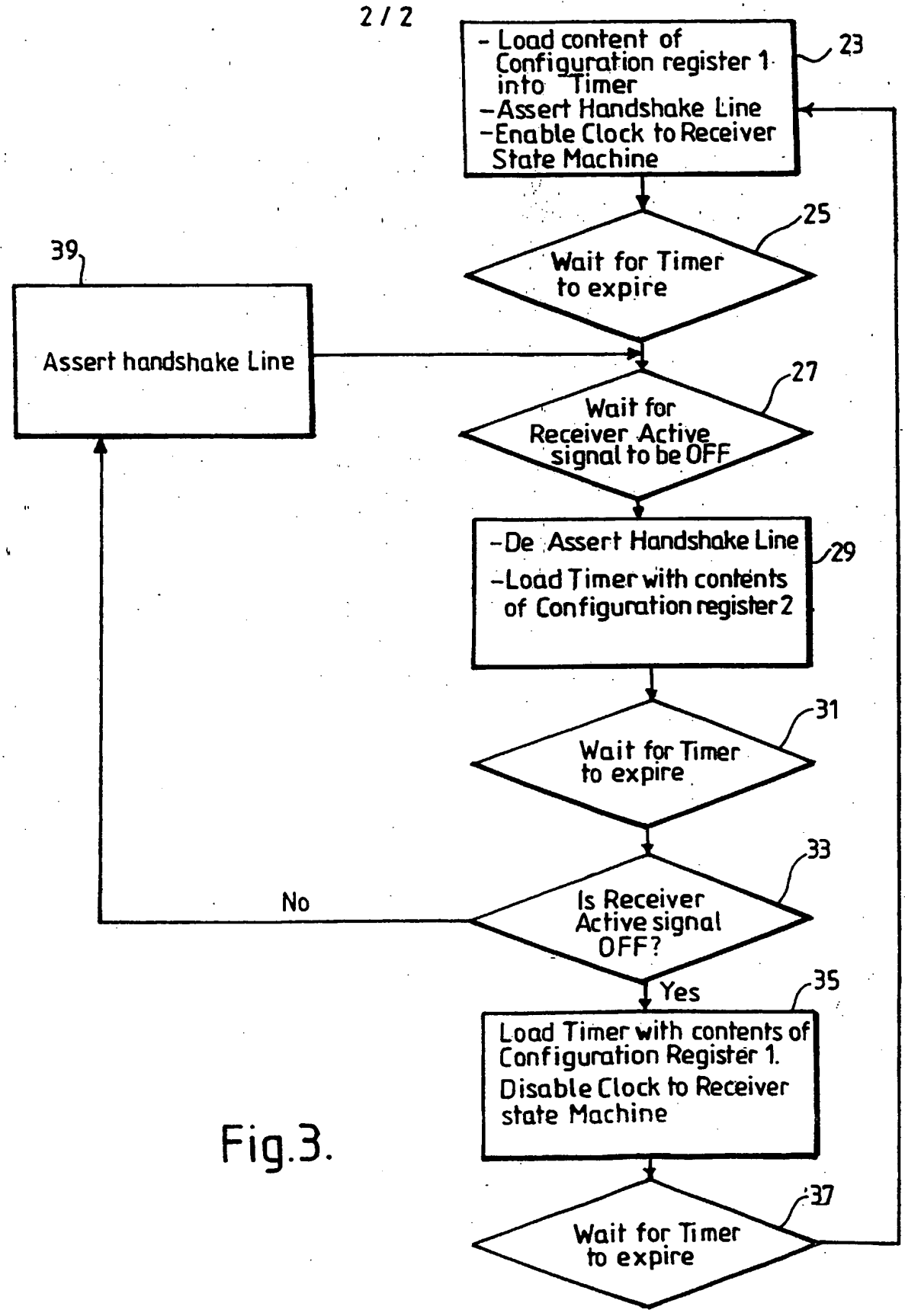
- Load content of Configuration register 1 into Timer
-Assert Handshake Line
-Enable Clock to Receiver State Machine
23
Wait for Timer to expire
25
39
Assert handshake Line
Wait for Receiver Active signal to be OFF
27
-De Assert Handshake Line
-Load Timer with contents of Configuration register 2
29
Wait for Timer to expire
31
Is Receiver Active signal OFF?
33
No
Yes
Load Timer with contents of Configuration Register 1.
Disable Clock to Receiver state Machine
35
Wait for Timer to expire
37

Fig.3.

being at, or below, the predetermined amount; and (iv) re-enabling the receiving means of the peripheral device when data is able to be transferred to the peripheral device.

Thus, the method enables a reduced power consumption by means of disabling the reception of data by the peripheral device if no data is to be transmitted over the data channel, effectively putting the peripheral in a low-power mode. This can be done by disabling the clock signals within the peripheral device until such time when data is ready to be transmitted over the data channel.

The method may further comprise sending a command signal from the peripheral device to the host communications device when the amount of transferred data is at, or below, the predetermined amount, the host communications device being configured to stop sending further data in response to receiving the command signal.

The data channel may include a communications bus and a handshake line, the handshake line being used to transmit the command signal from the peripheral device to the host communications device, and the communications bus being used to send data from the host communications device to the peripheral device. The data channel may use a combined communications bus which includes a handshake line as part of its configuration.

In the preferred embodiment, in an initial state, step (ii) is not performed until after a first predetermined time delay. Also, when it is determined that the amount of data being transferred is at, or below, the predetermined amount, step (ii) is repeated after a second predetermined time delay, step (iii) being performed only if the amount of data being transferred remains at or below the predetermined amount. Following step (iii), the receiving means of the peripheral device may remain disabled for a third predetermined time period, step (iv) being performed only after the third predetermined time period has completed.

Preferably, the predetermined amount of data being transferred is zero.

The control means can be further arranged to send a command signal to the host communications device when the amount of transferred data is at, or below, the predetermined threshold thereby to prevent further data being sent from the host communications device.

The peripheral device can further comprise a communications bus and a handshake line which are connected to the data channel, the control means being arranged to (i) transmit the command signal over the handshake line to the data channel, and (ii) receive data over the communications bus.

The control means can be arranged such that, in an initial state, it does not determine whether the amount of data being transferred is at, or below, the predetermined amount until after a first predetermined time delay. The control means may arranged such that, when it is determined that the amount of data being transferred is at, or below, the predetermined amount, the control means repeats this determination operation once again after a second predetermined time delay, the control means being arranged to perform the disabling operation only if the amount of data being transferred remains at or below the predetermined amount after the second predetermined time delay. The control means can be arranged to keep the receiving means disabled for a third predetermined time delay, and to re-enable the receiving means only after the third predetermined time period has completed.

Preferably, the control means is arranged such that the predetermined amount of data at which the receiving means is disabled is set to zero.

The invention will now be described, by way of example, with reference to the accompanying drawings, in which:

Figure 1 is a block diagram of a communications system including a host communications device and a Bluetooth peripheral device;

First, second and third configuration registers 15, 17, 19 are connected to the power save state machine 9. These configuration registers 15, 17, 19 contain respective first, second and third predetermined data values, the purpose of which will be discovered below.

The power save state machine 9 is configured to apply a signal to the handshake line 10 so as to indicate to the PDA 1 that data should or should not be sent to the Bluetooth peripheral device 3 over the data communications bus 8. The handshake line 10 is asserted to indicate that the Bluetooth peripheral device 3 can receive data, and de-asserted to indicate that the Bluetooth peripheral device should not receive data. Latency is allowed when the de-asserted signal is applied to account for certain registers of the PDA 1 (e.g. first-in first-out (FIFO) registers) which empty data from their 'stack' for a predetermined time period.

The power save state machine 9 operates according to a predetermined algorithm which will now be described in detail with reference to the flow chart of Figure 3. It will be appreciated that the algorithm can readily be realised in a computer program which can be downloaded to a peripheral communications device, such as the Bluetooth device 3 described in this embodiment.

Referring now to Figure 3, in an initial state 23, the power save state machine 9 loads the first predetermined data value into the timer 13 via input line 14. The handshake line 10 is asserted to indicate that data can be sent from the PDA 1 over the data communications bus 8. The clock is also enabled by means of applying a high 'clock enable' signal to the AND gate 21. The resultant clock signal is applied to the receiver state machine 11. The first predetermined data value stored in the timer 13 decrements when the handshake line 10 is asserted. The time taken for the timer 13 to reach zero is appropriately set to equal the maximum amount of time taken for the PDA 1 to start transmitting available data after the handshake line 10 is asserted. Accordingly, any inherent time lag in the system is accounted for. Thus, in the next step 25, the timer 13

in transferring data from the PDA 1 to the Bluetooth peripheral device. In this step, the Bluetooth peripheral device 3 enters a low power mode since the clock signal is disabled and no data is received. Once the timer reaches zero, in step 37, the algorithm returns to the initial state 23 and the process repeats as before.

The method and system described above enables the Bluetooth peripheral device 3 to effectively enter an ultra-low power mode in which clock devices associated with data transfer can be disabled when no data is required to be transmitted. Data loss is prevented through the use of a hardware handshake mechanism which stop the host computer from sending data whilst the peripheral is in the low power mode. Latency in the PDA 1 responding to a change in handshake signals is catered for.

As already mentioned, the algorithm of Figure 3 can be realised in a hardware state machine or in a software program. Indeed, a combination of hardware and software could be used. Whilst a communications system using the RS232 protocol has been described, the method finds equal application in other serial and parallel data transfer protocols.

6. A method according to any preceding claim, wherein following step (iii) the receiving means of the peripheral device remains disabled for a third predetermined time period, step (iv) being performed only after the third predetermined time period has completed.

7. A method according to any preceding claim, wherein the predetermined amount of data being transferred is zero data.

8. A method according to any preceding claim, wherein the peripheral device receives data using the RS232 protocol.

9. A computer program stored on a computer usable medium and comprising computer readable instructions for causing a processing means to execute the steps of the method according to any preceding claim.

10. A peripheral device for receiving data from a host communications device over a data channel, the peripheral device comprising: receiving means for processing received data; and control means arranged to (i) monitor the amount of data being received from the host communications device, (ii) determine when the amount of data being transferred is at, or below, a predetermined amount, (iii) disable the receiving means in response to the amount of received data being at, or below, the predetermined amount; and (iv) re-enable the receiving means when data is able to be transferred to the peripheral device.

11. A peripheral device according to claim 10, wherein the control means is further arranged to send a command signal to the host communications device when the amount of transferred data is at, or below, the predetermined threshold thereby to prevent further data being sent from the host communications device.

12. A peripheral device according to claim 11, further comprising a communications bus and a handshake line which are connected to the data channel, the

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**Application No:** GB 0206852.6 **Examiner:** Adam Tucker
**Claims searched:** 1-18 **Date of search:** 28 August 2002

## Patents Act 1977
## Search Report under Section 17

**Databases searched:**

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.T): G4H HRCA, H4L LECTH, LECTA, LECTW

Int Cl (Ed.7): G06F 1/32, H04B 1/16, H04M 1/73, H04Q 7/18, 7/32

Other: Online: WPI, EPODOC, PAJ, INSPEC

**Documents considered to be relevant:**

| Category | Identity of document and relevant passage | | Relevant to claims |
|---|---|---|---|
| A, E | WO 02/25826 A2 | Ericsson, See in particular page 11 lines 7-29 | - |
| X | WO 97/29553 A1 | Intel Corp., See in particular page 11 line 13-page 12 line 6 and page 14 lines 2-25 | 1, 7, 9, 10, 16 |
| X | WO 97/15913 A1 | Elonex Technologies, See in particular page 3 line 34-page 4 line 14, page 11 lines 18-28 and page 13 lines 9-24 | 1, 7-10, 16 |
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| X | US 5594672 | Hicks, See in particular the abstract, the summary of the invention | 1, 7-10, 16 |
| X | US 5477476 | Schanin et al., See whole document | 1, 4, 5, 7-10, 13, 14, 16 |

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